CLAIMS

What is claimed is:

1.   A method of fabricating an integrated circuit on a wafer using dual mask exposure lithography, comprising:

5   forming a photo resist layer over the wafer;

aligning the wafer with respect to a lithography system using a reference mark that is formed on the wafer;

exposing the photo resist layer with a first mask image defined by a first mask using the lithography system, the first mask image including a latent image

10   alignment mark that is transferred to the photo resist layer;

re-aligning the wafer with respect to the lithography system using the latent image alignment mark resulting from the exposure to the first mask image; and

exposing the photo resist layer with a second mask image defined by a

15   second mask using the lithography system.

2.   The method according to claim 1, further comprising developing the photo resist layer after exposure with both the first mask image and the second mask image.

3.   The method according to claim 2, further comprising using the

20   developed photo resist layer to protect a layer underlying the photo resist layer from at least one of etching, implantation and chemical reaction.

4.   The method according to claim 1, wherein the lithography system is selected from a step-and-repeat lithography system, a step-and-scan system and combinations thereof.

25   5.   The method according to claim 1, wherein the lithography system includes a first alignment sensor for tracking a location of the reference mark and

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a second alignment sensor for tracking a location of the latent image alignment mark.

6. The method according to claim 1, further comprising enhancing detectability of the latent image alignment mark to an alignment sensor.

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7. The method according to claim 6, wherein the enhancing includes adding a compound to the photo resist layer during photo resist formation such that the photo resist layer changes appearance in locations exposed to a threshold amount of energy as defined by the first mask image.

8. The method according to claim 6, wherein the enhancing includes
10 developing a portion of the photo resist layer after exposure by the first mask image to establish a latent image alignment mark edge in the photo resist layer.

9. The method according to claim 8, wherein the photo resist layer includes at least two sublayers and the developed portion of the photo resist layer includes a top layer of the sublayers.

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10. The method according to claim 1, wherein the photo resist layer includes at least two sublayers and exposure by the first mask image results in latent image alignment mark detectability in at least a top one of the sublayers.

11. The method according to claim 1, further comprising enhancing detectability of the latent image alignment mark by increasing exposure of the
20 latent image alignment mark with the first mask image.

12. The method according to claim 11, wherein increasing the exposure includes exposing at least twice with the first mask.

13. The method according to claim 11, wherein increasing the exposure includes exposing with an overlapping exposure.

14.   The method according to claim 1, wherein one of the first mask image and the second mask image defines critical dimension structures and the other of the first mask image and the second mask image defines non-critical dimension structures.

5   15.   The method according to claim 1, wherein one of the first mask image and the second mask image defines edges in a first direction and the other of the first mask image and the second mask image defines edges in a second direction transverse to the first direction.

16.   The method according to claim 1, further including at least partially 10   developing the photo resist layer between exposing with the first mask image and the second mask image.

17.   The method according to claim 1, wherein the first mask image and the second mask image create a composite mask image on the photo resist layer.

15   18.   A method of fabricating a hard mask layer on a wafer using dual mask exposure lithography, comprising:

forming a first photo resist layer over a layer of hard mask material that is formed over the wafer;

aligning the wafer with respect to a lithography system using a reference 20   mark that is formed on the wafer;

exposing the first photo resist layer with a first mask image defined by a first mask using the lithography system, the first mask image including a latent image alignment mark that is transferred to the photo resist layer;

developing the first photo resist layer;

25   etching the hard mask material layer to transfer a layout of the first mask image to the hard mask material layer, the transferred layout including the latent image alignment mark;

re-aligning the wafer with respect to the lithography system using the latent image alignment mark; and

exposing the wafer with a second mask image defined by a second mask using the lithography system.

5   19.   The method according to claim 18, further comprising developing the photo resist and etching the hard mask material layer to transfer a layout of the second mask image to the hard mask material layer.

20.   The method according to claim 18, further comprising forming a second photo resist layer over the layer of hard mask material after etching of the

10   hard mask material layer to transfer the layout of the first mask image to the hard mask material layer.

21.   The method according to claim 20, further comprising removing the first photo resist layer before forming the second photo resist layer.

22.   The method according to claim 18, wherein the lithography system

15   is selected from a step-and-repeat lithography system, a step-and-scan system and combinations thereof.

23.   The method according to claim 18, wherein the lithography system includes a first alignment sensor for tracking a location of the reference mark and a second alignment sensor for tracking a location of the latent image alignment

20   mark.